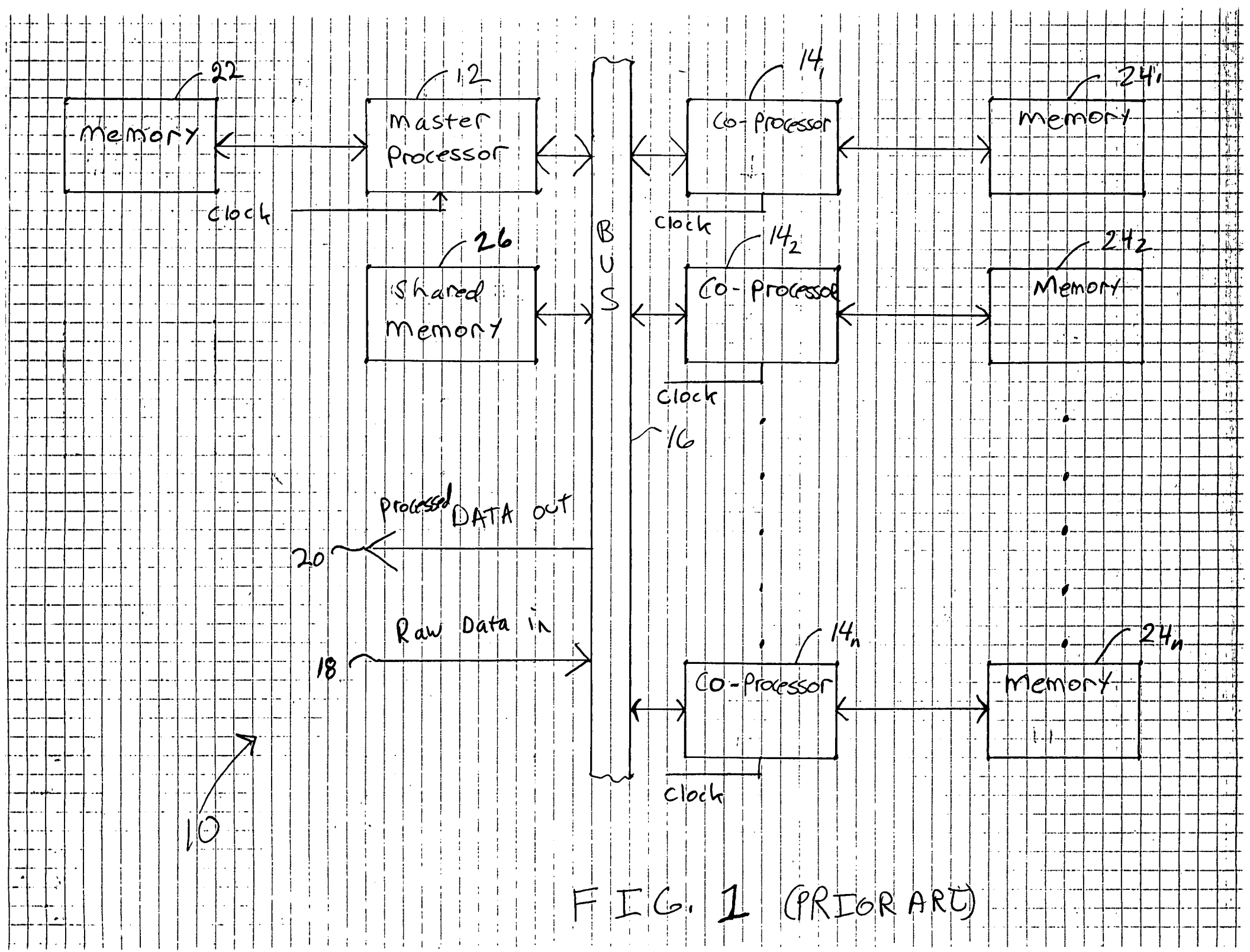

FIG. 1 (PRIOR ART)

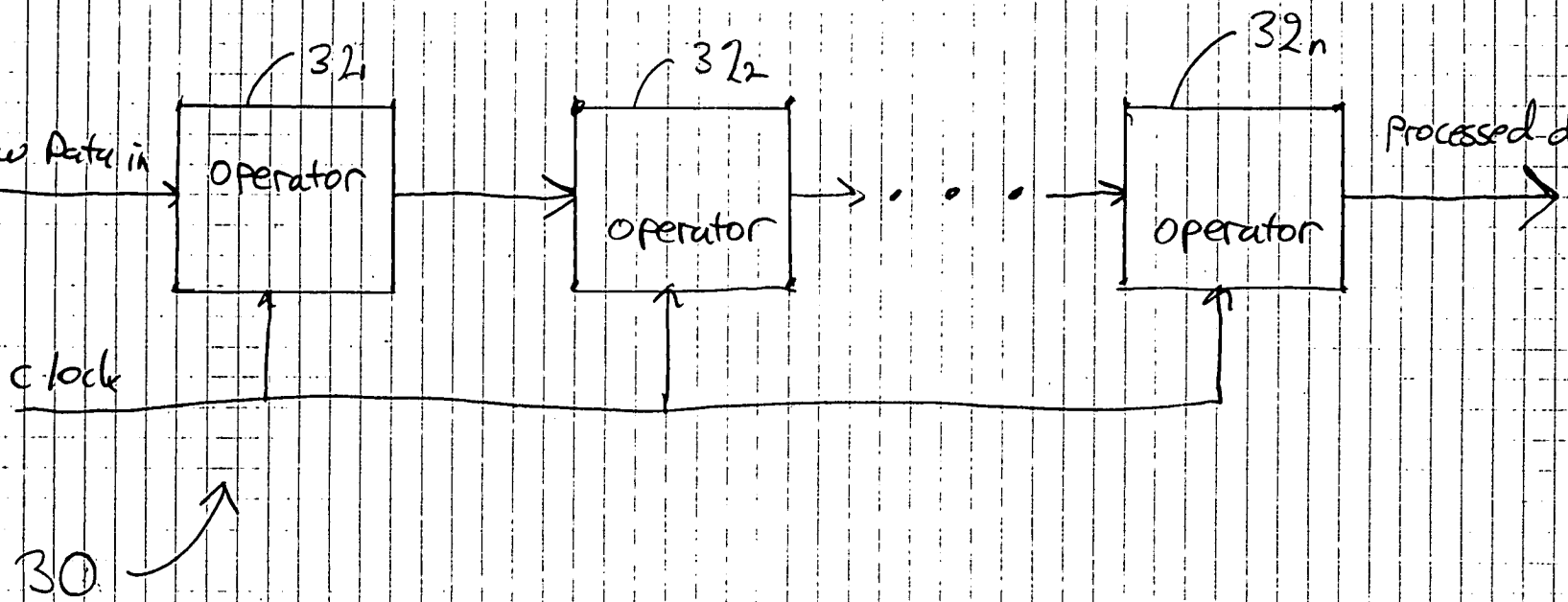
32₁
32₂
32n
Raw Data in
operator
operator
operator
processed data out
clock
30

FIG. 2

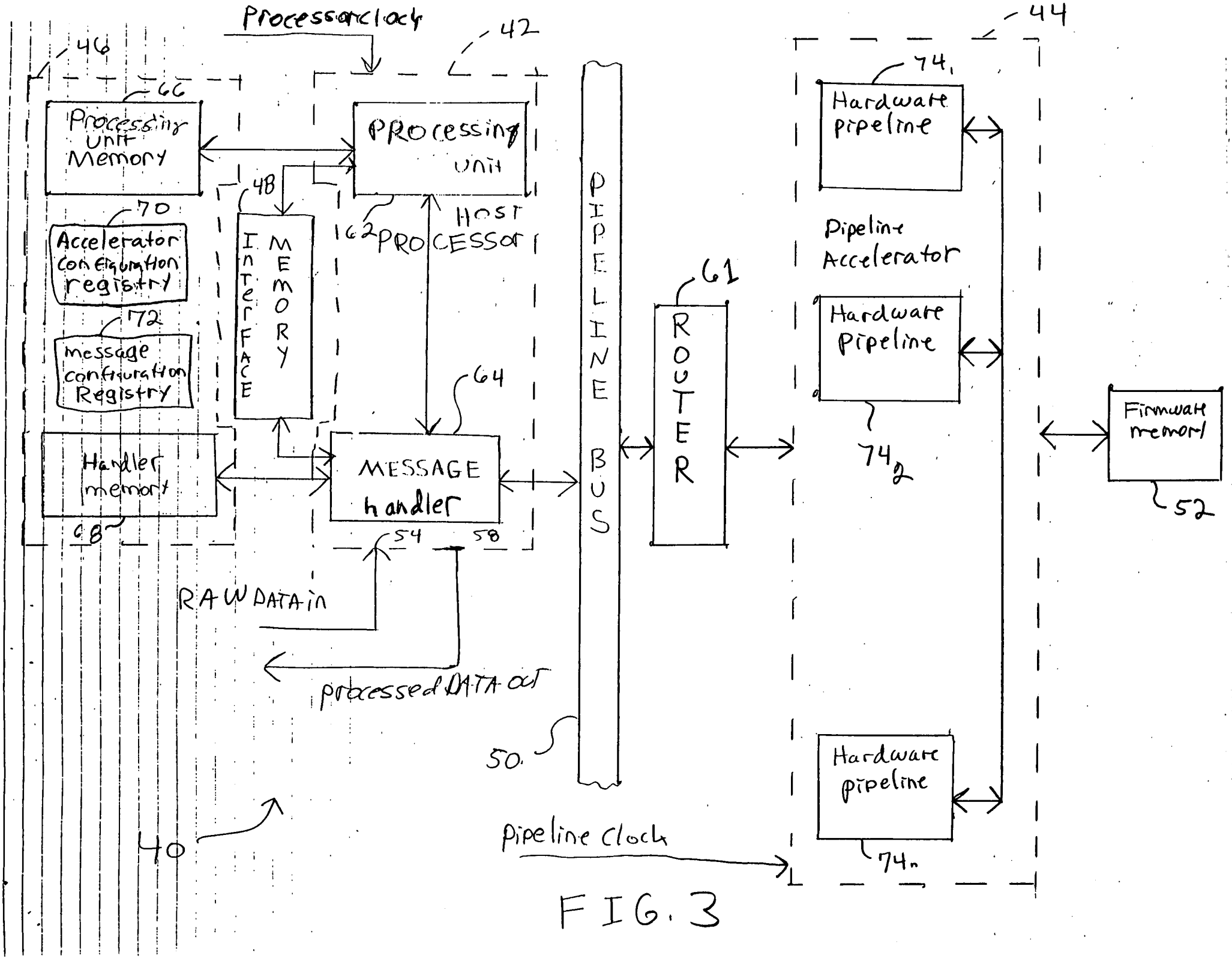
Processor clock
42
44
46
66
Processing unit Memory
PROcessing unit
74,
Hardware pipeline
48
INTERFACE MEMORY
62 PROCESSOR
HOST
Pipeline Accelerator
70
Accelerator configuration registry
172
message configuration Registry
PIPELINE BUS
61
ROUTER
Hardware pipeline
74₂
Firmware memory
52
64
Handler memory
MESSAGE handler
68
54
58
RAW DATA in
processed DATA out
50
Hardware pipeline
74n
40
Pipeline clock

FIG. 3

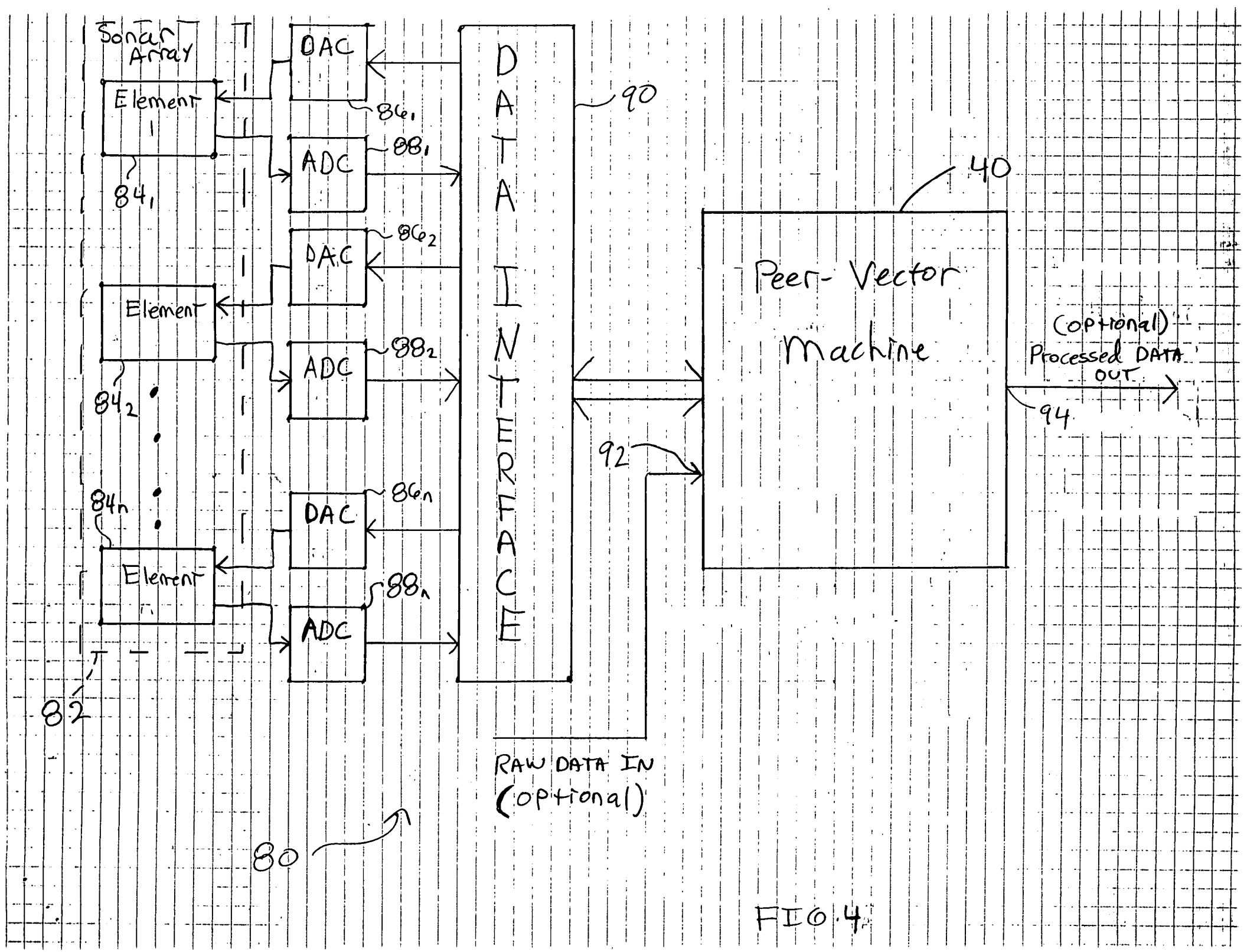
Sonar Array
Element
Element
Element
DAC
ADC
DAC
ADC
DAC
ADC
DATA INTERFACE
Peer-Vector Machine
(optional) Processed DATA OUT
RAW DATA IN (optional)
82
80
84₁
84₂
84n
86₁
88₁
86₂
88₂
86n
88n
90
92
94
40

FIG. 4